## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

## REPLY TO RESTRICTION REQUIREMENT DATED 01/16/2008

Atty. Docket No. SUZU1720

Applicant:

Takeshi Ishigaki

Application Number

10/586,951

Filed

07/25/2006

For

Semiconductor Integrated Circuit Device and Method of Outputting Signals on Semiconductor

**Integrated Circuit** 

Group Art Unit

Examiner

4125

Rojas, Daniel E.

Confirmation No. 3389

Commissioner of Patents

P.O. Box 1450

Alexandria, VA 22313

Dear Sir:

## Certificate of Transmission Under 37 C.F.R. § 1.8

I hereby certify that this correspondence is being deposited electronically using the United States Patent Office EFS-Web system on 2-6-2008.

C/ /

STAW SHOW KERBY

The Examiner states that restriction is required under 35 U.S.C. § 121 to one of the following inventions:

Group I:

Claims 1-5 and 20, drawn to a semiconductor integrated circuit device comprising a semiconductor substrate, counter, global reset circuit, local reset circuit and a first circuit; or

Group II:

Claims 6-10, drawn to a semiconductor integrated circuit device comprising a semiconductor substrate having a first and second area, plurality of counters in the first and second areas, a first clock circuit in the first area, a first circuit in the first area, a second clock circuit and a second circuit in the second area; or

Group III:

Claims 11-19, drawn to a semiconductor integrated circuit device comprising a semiconductor substrate having a first area and a second area, a first counter in the second area, a first clock circuit, a first circuit in the second area, a first clock signal, and a second clock signal.

Applicant elects to prosecute Group II without traverse.

Applicant does not believe any fees and due and owing. If any fees are required, or if any amounts have been overpaid, please appropriately charge or credit those fees to Deposit Account No. 50-3183 of Sprinkle IP Law Group.

Respectfully submitted,

Sprinkle IP Law Group

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